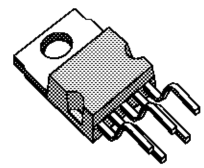
L4947
L4947R

5V-0.5A VERY LOW DROP REGULATOR WITH RESET

- PRECISE OUTPUT VOLTAGE (5V ± 4%) OVER FULL TEMPERATURE RANGE (– 40 / 125 °C)
- VERY LOW VOLTAGE DROP (0.75Vmax) OVER FULL T RANGE
- OUTPUT CURRENT UP TO 500mA
- RESET FUNCTION
- POWER-ON RESET DELAY PULSE DEFINED BY THE EXTERNAL CAPACITOR
- + 80V LOAD DUMP PROTECTION
- – 80V LOAD DUMP PROTECTION
- REVERSE VOLTAGE PROTECTION
- SHORT CIRCUIT PROTECTION AND THERMAL SHUT-DOWN (with hysteresis)
- LOW START UP CURRENT



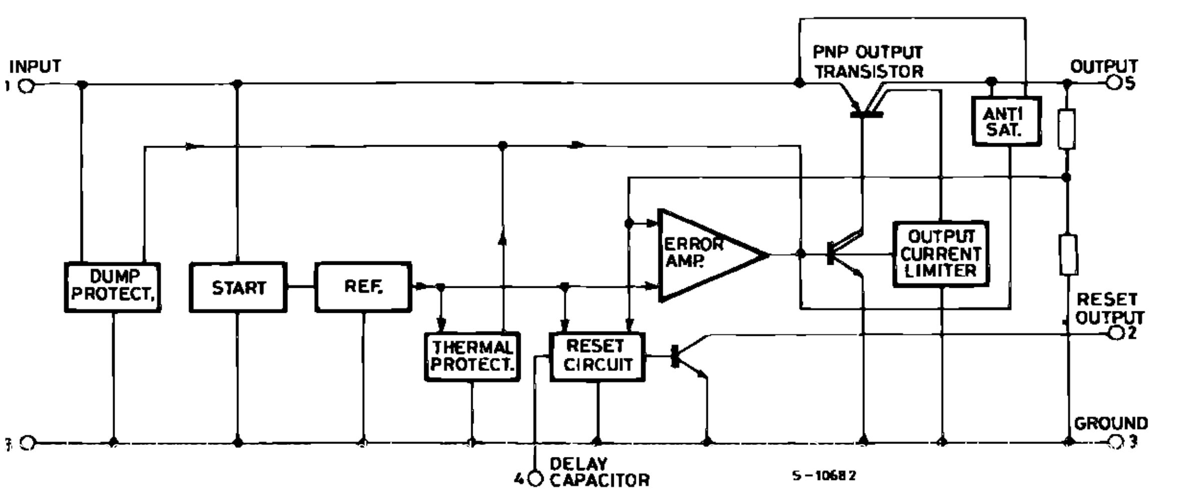
Pentawatt

ORDERING NUMBER: L4947
L4947R

DESCRIPTION

The L4947/L4947R is a monolithic integrated circuit in Pentawatt package specially designed to provide a stabilized supply voltage for automotive and industrial electronic systems. Thanks to its very low voltage drop, in automotive applications the L4947/L4947R can work correctly even during the cranking phase, when the battery voltage could fall as low as 6V. Furthermore, it incorporates a complete range of protection circuits against the dangerous overvoltages always present on the battery rail of the car. The reset function makes the device particularly suited to supply microprocessor based systems : a signal is available (after an externally programmable delay) to reset the microprocessor at power-on phase ; at power-off, this signal becomes low inhibiting the microprocessor.

BLOCK DIAGRAM

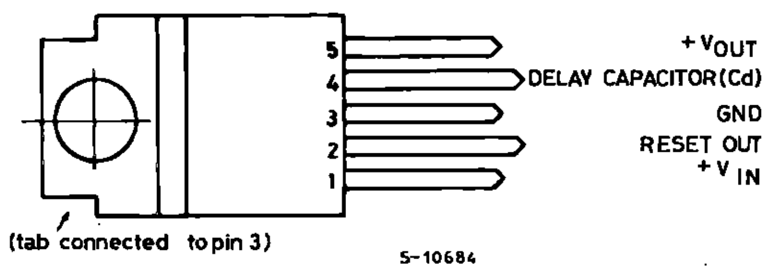


ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage DC Reverse Input Voltage Transient Input Overvoltages : Load Dump : 5ms ≤ t_{rise} ≤ 10ms τ_f Fall Time Constant = 100ms R_{SOURCE} ≥ 0.5Ω Field Decay : 5ms ≤ t_{fall} ≤ 10ms, R_{SOURCE} ≥ 10Ω τ_r Rise Time Constant = 33ms Low Energy Spike : t_{rise} = 1µs, t_{fall} = 500µs, R_{SOURCE} ≥ 10Ω f_r Repetition Frequency = 5Hz	35 – 18 80 – 80 ± 100	V V V V V
V_R	Reset Output Voltage	35	V
T_J, T_{stg}	Junction and Storage Temperature Range	– 55 to 150	°C

Note: The circuit is ESD protected according to MIL-STD-883C.

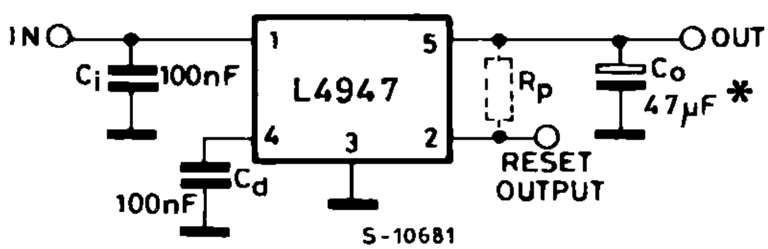
PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case Max	3.5	°C/W

TEST CIRCUIT



(*) Min. 20µF, ESR < 10Ω over full temperature range R_P (pull up resistor) and R_L (load) are both equal to 1KΩ.

ELECTRICAL CHARACTERISTICS (refer to the test circuit, V_i = 14. 4V, C_o = 47μF, ESR < 10Ω, R_p = 1KΩ, R_L = 1KΩ, –40°C ≤ T_J ≤ 125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	I_o = 0mA to 500mA Over Full T Range T_J = 25°C	4.80 4.90	5.00 5.00	5.20 5.10	V V
V_i	Operating Input Voltage	I_o = 0mA to (*) 500mA	6		26	V
ΔV_o	Line Regulation	V_i = 6V to 26V ; I_o = 5mA		2	10	mV
ΔV_o	Load Regulation	I_o = 5mA to 500mA		15	60	mV
$V_i – V_o$	Dropout Voltage	I_o = 500mA, T_J = 25°C Over Full T Range		0.40	0.55 0.75	V V
I_q	Quiescent Current	I_o = 0mA, T_J = 25°C I_o = 0mA Over Full T I_o = 500mA Over Full T		5 6.5 110	10 13 180	mA mA mA
$\frac{\Delta V_o}{T}$	Temperature Output Voltage Drift			– 0.5		mV/°C
SVR	Supply Volt. Rej.	I_o = 350mA ; f = 120Hz C_o = 100μF ; V_i = 12V ± $5V_{pp}$	50	60		dB
I_{sc}	Output Short Circuit Current		0.50	0.80	1.50	A
V_R	Reset Output Saturation Voltage	1.5V < V_o < $V_{RT\ (off)}$, I_R = 1.6mA 3.0V < V_o < $V_{RT\ (off)}$, I_R = 8mA			0.40 0.40	V V
I_R	Reset Output Leakage Current	V_O in Regulation, V_R = 5V			50	μA
$V_{RT\ peak}$	Power On-Off Reset out Peak Voltage	1KΩ Reset Pull-up to V_o, T_J = 25°C		0.50	0.80	V
$V_{RT\ (off)}$	Power OFF V_o Threshold	T_J = 25°C **L4947:** V_o @ Reset Out H to L Transition	 4.70 4.75	 Vo–0.15		 V V
		L4947R: V_o @ Reset Out H to L Transition	4.55	Vo–0.30		V
$V_{RT\ (on)}$	Power ON V_o Threshold	V_o @ Reset Out L to H Transition		$V_{RT\ (off)}$ + 0.05	V_o – 0.04	V
V_{Hyst}	Power ON-Off Hysteresis	$V_{RT\ (on)} – V_{RT\ (off)}$		0.05		V
V_d	Delay Comparator Threshold	V_d @ Reset Out L to H Transition	3.65	4.00	4.35	V
		V_d @ Reset Out H to L Transition	3.20	3.55	3.90	V
V_{dH}	Delay Comparator Hysteresis			0.45		V
I_d	Delay Capacitor Charging Current	V_d = 3V, T_J = 25°C		20		/μA
V_{disch}	Delay Capacitor Discharge Voltage	V_o < $V_{RT\ (off)}$		0.55	1.20	V
T_d	Power on Reset Delay Time	C_d = 100nF, T_J = 25°C	10	20	30	ms

(*) For a DC voltage 26 < V_i < 37V the device is not operating

FUNCTIONAL DESCRIPTION

The L4947/L4947R is a very low drop 5V/0.5A voltage regulator provided with a reset function and therefore particularly suited to meet the requirements of supplying the microprocessor systems used in automotive and industrial applications.

The block diagram shows the basic structure of the device : the reference, the error amplifier, the driver, the power PNP, the protection and reset functions.

The power stage is a Lateral PNP transistor which allows a very low dropout voltage (typ. 400mV at T_J = 25°C, max. 750mV over the full temperature range @ I_O = 500mA). The typical curve of the dropout voltage as a function of the junction temperature is shown in Fig. 1 : that is the worst case, where I_O = 500mA.

The current consumption of the device (quiescent current) is maximum 13mA - over full T - when no load current is required.

The internal antisaturation circuit allows a drastic reduction in the current peak which takes place during the start up.

The reset function supervises the regulator output voltage inhibiting the microprocessor when the device is out of regulation and resetting it at the power-on after a settable delay. The reset is LOW when the output voltage value is lower than the reset threshold voltage. At the power-on phase the output voltage increases (see Fig. 2) and - when it reaches the power-on V_O threshold V_{RT} (On) - the reset output becomes HIGH after a delay time set by the external capacitor C_d. At the power-off the output voltage decreases : at the $V_{RT(Off)}$ threshold value (V_O-0.15V typ. for L4947 and V_O-0.3V typ. for L4947R value) the reset output instantaneously goes down (LOW status) inhibiting the microprocessor. The typical power on-off hysteresis is 50mV.

Figure 1: Typical Dropout Voltage vs. T_j (I_o = 500mA).

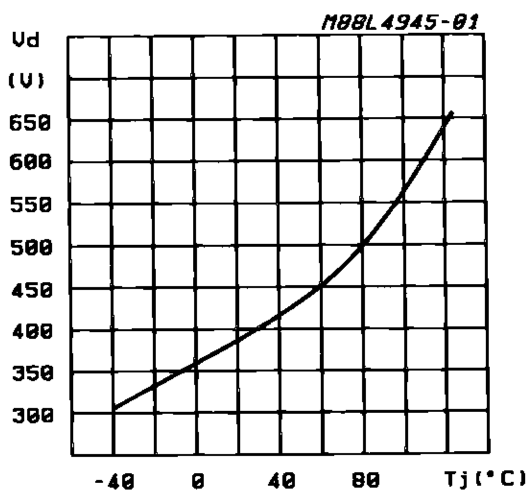
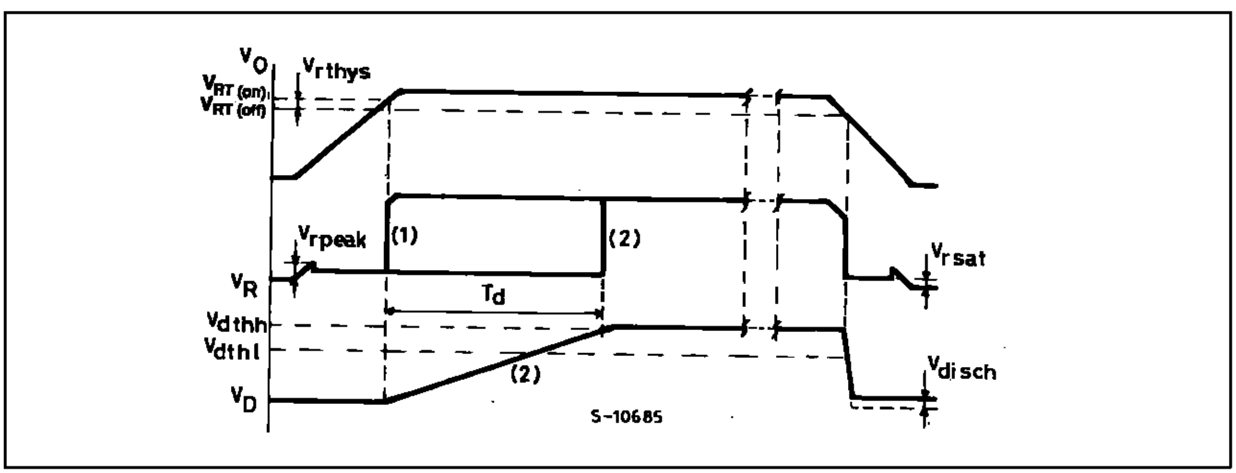


Figure 2: Reset Waveforms:
(1) Without External Capacitor C_d.
(2) With External Capacitor C_d.



The three gain stages (operational amplifier, driver and power PNP) require the external capacitor (C_{omin} = 20µF) to guarantee the global stability of the system.

Load dump and field decay protections (± 80V), reverse voltage (– 18V) and short circuit protection, thermal shutdown are the main features that make the L4947/L4947R specially suitable for applications in the automotive enviroment.

EXTERNAL COMPENSATION

Since the purpose of a voltage regulator is to supply and load variations, the open loop gain of the regulator must be very high at low frequencies. This may cause instability as a result of the various poles present in the loop. To avoid this instability dominant pole compensation is used to reduce phase shift due to other poles at the unity gain frequency. The lower the frequency of these others poles at the unity gain frequency. The lower the frequency of these other poles, the greater must be capacitor esed to create the dominant pole for the same DC gain.

Where the output transistor is a lateral PNP type there is a pole in the regulation loop at a frequencybtoo low to be compensated by a capacitor which can be integrated. An external compensation is therefore necessary so a very high value capacitor must be connected from the output to ground.

The paeassitic equivalent series resistance of the capacitor used adds a zero to the regulation loop. This zero may compromise the stability of the system since its effect tends to cancel the effect of the pole added. In regulators this ESR must be less than 3Ω and the minimum capacitor value is 47µF.

PENTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G		3.4		0.126	0.134	0.142
G1		6.8		0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152

